Amendments to the Claims:

The following listing of claims replaces all prior versions and listings of claims in the application:

1. (canceled)

2. (canceled)

3. (original) A method of fabricating a flash memory comprising:

forming a cell region for memory operation and a peripheral region including a subsidiary circuit for memory operation on a silicon substrate;

amorphizing the surface of the cell region by implanting ions into the cell region;

depositing a pad oxide layer and a pad nitride layer in sequence over the cell region and the peripheral region;

forming a photoresist pattern over each of the pad nitride layer in the cell region and the peripheral region;

removing at least a portion of the pad oxide layer and the pad nitride layer through an etching process using the photoresist pattern as a mask, wherein the etching process is stopped when the surface of the substrate in the cell region is exposed and, at the same time, the substrate in the peripheral region is etched by an appropriate depth;

removing the photoresist pattern; and

performing an etching process using the pad nitride layer etched as a mask so that a relatively shallow cell trench area is formed in the cell region and a relatively deep peripheral trench area is formed in the peripheral region.

4. (original) The method as defined by claim 3, wherein the ion concentration used to perform the ion implantation is between about 1E14 and 5E14.

5. (previously presented) The method as defined by claim 3, wherein the implanted ion is one of Ge and one selected from group IV elements.

6. (original) The method as defined by claim 3, wherein the ion implantation is performed using an inert gas such as Ar, Xe, or Kr.

7. (canceled)

8. (canceled)

9. (canceled)